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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/598,580	04/18/2008	Jeffrey H. Reed	01640454AA	7355

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WHITHAM, CURTIS & CHRISTOFFERSON & COOK, P.C.
11491 SUNSET HILLS ROAD
SUITE 340
RESTON, VA 20190

EXAMINER	
JORDAN, KIMBERLY L	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/598,580	REED ET AL.	
	Examiner	Art Unit	
	Kimberly Jordan	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 September 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/05/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is the initial Office action based on the application filed on April 18, 2008.

2. Claims 1-8 are pending and have been examined.

3. Claims 1-8 do not meet the 3-prong test and are not presumed to invoke 35 U.S.C. 112, sixth paragraph. Claim 1 contains the limitation "integrated circuit means" which does not meat prong (C) of the 3-prong test, "(C) the phrase "means for " or "step for " must not be modified by sufficient structure, material, or acts for achieving the specified function" (MPEP 2181).

Information Disclosure Statement

4. The Information Disclosure Statement filed on 09/05/2006 has been considered. An initialed copy of Form 1449 is enclosed herewith.

Drawings

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description:

- Figure 3, reference number 370

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet

submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Double Patenting

6. Claims 1-8 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-16 of copending Application No. 10/598,575. Although the conflicting claims are not identical, they are not patentably distinct from each other because the examined application claim is anticipated by the reference claims. See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); and In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985). In determining whether a nonstatutory basis exists for a double patenting rejection, the first question to be asked is — does any claim in the application define an invention that is anticipated by, or is merely an obvious variation of, an invention claimed in the patent? If the answer is yes, then an "obviousness-type" nonstatutory double patenting rejection may be appropriate. See MPEP 804 (II)(B)(1) Nonstatutory Double Patenting, Obvious-Type. The difference between the inventions defined by the conflicting claims is that the object request broker (ORB) of the instant application is simply middleware in the reference application. The examined application claim is anticipated by the reference claims in copending Application No. 10/598,575 because all the features recited in claims 1-8 of this application can also be found in claims 1-8 and 9-16, respectively of the reference application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. **Claims 1-4 and 6-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Pucker et al. (*Extending the SCA Core Framework Inside the Modem Architecture of a Software Defined Radio)**, hereinafter Pucker, in view of **Applicant Admitted Prior Art**, hereinafter APA.

Regarding **Claim 1,** Pucker discloses:

- *A hardware Object Request Broker (ORB) on a chip for controlling data transfer between embedded resources in a device* (see at least Figure 4; Figure 5)
- *first integrated circuit means for separating a functionality of said ORB into a control interface and a data interface, there being a...data interface for each of said object and each of said embedded resources; third integrated circuit means for constructing said data interfaces for said embedded resources outside said general purpose processor, such that said data transfer, under control of said object exercised through said second integrated circuit means, occurs directly between said embedded resources without going through said general purpose processor* (see at least Figure 3; Figure 5; Abstract, "This article illustrates the application of the SCA core framework for these types of modem architectures, including aggregating devices in support of direct hardware interconnects between components and the incorporation of a switched fabric communications infrastructure within the overall modem architecture."; Page S22, Paragraph 1, "Support for the SCA core framework within this type of architecture requires that each of the processing devices within the radio be exposed to the CORBA-based logical software bus. This bus is used to set up and tear down software components on these devices, and to connect and control these software components through well-defined CORBA Interface Definition Language (IDL) interfaces. Processing devices such as FPGAs and DSPs that do not support CORBA-enabled communications each require an SCA logical device adaptor that resides on a CORBA-enabled processor and acts as a proxy for the non-

CORBA-enabled device within the confines of the core framework. These logical devices form a bridge between the SCA logical software bus and hardware-specific application programming interfaces (APIs)."; Page S22, Paragraph 4, "An executable logical device running on the modem GPP to act as a software proxy for the FPGA. This device will be used to load (since an executable logical device is also a loadable logical device) an application resource targeted to the FPGA. Such a resource will consist of a firmware core to be loaded onto the FPGA itself and optionally a controller or proxy for the FPGA core to be executed on the GPP.")

However, Pucker does not explicitly disclose, but APA discloses:

- *second integrated circuit means for constructing said control interfaces within said general purpose processor of said device* (see at least APA, Figure 2, reference 255, device drivers are the control interface);
- *said ORB functionality enabling a software object resident on a general purpose processor of said device to transfer data between said embedded resources* (see at least APA, Figure 2), *there being a control interface...for each of said object and each of said embedded resources* (see at least APA, Figure 2, reference 255, device drivers are the control interface)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Pucker's direct connection between devices by incorporating the teachings of APA. APA simply provides the state of the art at the time of the invention as related to SCA standards and software radios. Pucker provides "...techniques for mapping the SCA

onto…hardware in a manner that maintains the benefits of SCA while providing the required performance to support advanced waveforms" (Abstract).

Regarding **Claim 2,** the rejection of Claim 1 is incorporated. However, Pucker does not explicitly disclose, but APA discloses:

- *wherein said respective control interfaces for each of said embedded resources are implemented using device drivers of said respective embedded resources* (see at least APA, Figure 2, reference number 255, device drivers are the control interface)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Pucker's direct connection between devices by incorporating the teachings of APA for the reasons listed above.

Regarding **Claim 3,** the rejection of Claim 1 is incorporated, and Pucker further discloses:

- *wherein said respective data interfaces for each of said embedded resources are each connected to a switch matrix, said switch matrix being external to said general purpose processor and serving to connect said embedded resources* (see at least Figure 5; Page S24, Section Switched Fabric Interconnects, Paragraph 1, "The need to support cumulative logical devices in the radio core framework component deployment to provide support for low-latency connections between critical processing elements inherently limits the flexibility of the radio

architecture, and may lead to an increase in the overall cost of the radio platform. One answer to this problem that has been discussed in the literature [6, 7] is to incorporate a high-speed switched data fabric, such as serial RapidIO, between the processing elements, as shown in Fig. 5.")

Regarding **Claim 4,** the rejection of Claim 3 is incorporated, and Pucker further discloses:

- *wherein said switch matrix is implemented as a connection fabric* (see at least Figure 5)

Regarding **Claim 6,** the rejection of Claim 1 is incorporated, and Pucker further discloses:

- *wherein said device is a software defined radio* (see at least Abstract, "Extension of the SCA core framework inside of the modem architecture of a software defined radio requires special consideration for managing the non-CORBA-enabled devices."), *said given system is the Joint Tactical Radio System, and said ORB is compliant with Software Communications Architecture (SCA)* (see at least Page S21, Paragraph 1, "A key enabler for software defined radio (SDR) technology is the Software Communications Architecture (SCA) developed by the Modular Software-Programmable Radio Consortium (MSRC) under contract to the Joint Tactical Radio System (JTRS) Program Office [1].")

Regarding **Claim 7,** the rejection of Claim 3 is incorporated, and Pucker further discloses:

- *wherein one of said embedded resources is a Field Programmable Gate Array (FPGA)* (see at least Figure 5)

Regarding **Claim 8,** the rejection of Claim 7 is incorporated, and Pucker further discloses:

- *fourth integrated circuit means for creating an Interface Description Language (IDL) description of a raw interface of said FPGA; fifth integrated circuit means for generating from said IDL a description of an interface between a core functionality of said FPGA and said switch matrix, and a description of a controller for performing said core functionality; and sixth integrated circuit means for integrating said core functionality interface into said data interface of said FPGA, and integrating said controller into said control interface of said FPGA* (see at least Page S24, Section Switched Fabric Interconnects, Paragraph 2, "Core framework support for a switched fabric interconnect is provided through the logical devices for each processing element. Each logical device defines one or more connections between the processing device it represents and the switched fabric through which it wishes to communicate. Connections between application software components are then made via the logical devices on which they are loaded."; Page S25, Paragraphs 2-5; Figure 3; Figure 5; Abstract, "This article illustrates the application of the SCA core framework for these types of modem

architectures, including aggregating devices in support of direct hardware interconnects between components and the incorporation of a switched fabric communications infrastructure within the overall modem architecture."; Page S22, Paragraph 1, "Support for the SCA core framework within this type of architecture requires that each of the processing devices within the radio be exposed to the CORBA-based logical software bus. This bus is used to set up and tear down software components on these devices, and to connect and control these software components through well-defined CORBA Interface Definition Language (IDL) interfaces. Processing devices such as FPGAs and DSPs that do not support CORBA-enabled communications each require an SCA logical device adaptor that resides on a CORBA-enabled processor and acts as a proxy for the non-CORBA-enabled device within the confines of the core framework. These logical devices form a bridge between the SCA logical software bus and hardware-specific application programming interfaces (APIs)."; Page S22, Paragraph 4, "An executable logical device running on the modem GPP to act as a software proxy for the FPGA. This device will be used to load (since an executable logical device is also a loadable logical device) an application resource targeted to the FPGA. Such a resource will consist of a firmware core to be loaded onto the FPGA itself and optionally a controller or proxy for the FPGA core to be executed on the GPP.")

10. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Pucker et al. (*Extending the SCA Core Framework Inside the Modem Architecture of a Software Defined Radio*)**, hereinafter Pucker, in view of **Applicant Admitted Prior Art**, hereinafter APA, as applied to claim 3 above, and further in view of **Murotake (*Use of Switched Fabrics in Implementation of Software Defined Radio Smart Antenna and Interference Cancellation Signal Processing*)**.

Regarding **Claim 5,** the rejection of Claim 3 is incorporated. However Pucker and APA do not explicitly disclose, but Murotake discloses:

- *wherein said switch matrix is implemented as a shared memory* (see at least Page 3, Section 4, Paragraph 2, "Early crossbar fabrics were based on "parallel" I/O fabrics. For example, a 32-bit, 40 MHz, 6-port crossbar switch architecture (RACEway Interlink) was introduced by Mercury Computer Systems, Inc. and standardized as ANSI/VITA 5-1994. RACEway is a circuit-switched architecture for embedded multi-processor systems employing a Globally Shared Memory (GSM).")

Therefore, it would have also been obvious to one of ordinary skill in the art at the time of the invention to modify Pucker and APA's direct connection between devices by incorporating the teachings of Murotake. Murotake states that switched fabrics may be used to connect devices in a software radio and also states that shared memories have been used in embedded multi-processor systems as well. Murotake provides an ideal connection implementation for software radios (Abstract).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bickle et al. discloses a radio software system with a middleware layer. Haji-Aghajani et al. discloses a framework that allows an application to be developed independent of the chip and dependency is built in as part of the framework of the FPD. Pucker discloses techniques for mapping the SCA onto such hardware in a manner that maintains the benefits of SCA while providing the required performance to support advanced waveforms.

12. Any inquiry of a general nature or relating to the status of this application or concerning this communication or earlier communications from the examiner should be directed to Kimberly Jordan whose telephone number is 571-270-5481. The examiner can normally be reached on Monday-Friday 9:30am-5pm EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on 571-272-6799.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kimberly Jordan/
Examiner, Art Unit 2194

/Hyung S. SOUGH/

Supervisory Patent Examiner, Art Unit 2194
August 27, 2010